The opinion in support of the decision being entered today
was **not** written for publication and
is **not** binding precedent of the Board.

Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TOSHIRO HIRAMOTO and MAKOTO TAKAMIYA

Appeal No. 2005-0753
Application No. 09/389,321

ON BRIEF[1]

Before: THOMAS, BLANKENSHIP and NAPPI, **Administrative Patent Judges**.

NAPPI, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 of the final rejection of claims 1 through 12. For the reasons stated *infra* we will not sustain the examiner's rejection of these claims.

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[1] The panel vacated the oral hearing scheduled for June 8, 2005, as the panel decided during a pre-hearing conference that the examiner's rejection would not be sustained.

Invention

The invention relates to a MOS transistor where the threshold voltage can be controlled. The MOS transistor comprises a Silicon-on-Insulator (SOI) device, which includes a substrate of semi-conductive material, a single crystal layer and an insulating layer between the two. The single crystal layer is formed with a source region, a drain region and a surrounded region, which includes a depletion layer, with a composition surface in contact with the insulating layer. See pages 4 and 5 of appellants' specification.

Claim 1 is representative of the invention and reproduced below:

> 1. A MOS transistor with a controlled threshold voltage comprising:
> a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-conducting material and an insulating layer interposed between said substrate and said single crystal layer,
> said single crystal layer being formed therein with a source region, a drain region and a surrounded region surrounded by said source region and said drain region,
> said surround region including a depletion layer having a composition surface which is in contact with said insulating layer,
> said MOS transistor comprising an EIB-MOS transistor of which said substrate is adapted to be applied with a voltage of a first polarity for inducing charges of a second polarity over said composition surface of the surround region.

References

The references relied upon by the examiner are:

Burr	6,100,567	Aug. 8, 2000 (filed Jun. 11, 1998)
Warashina et al. (Warashina)	5,698,885	Dec. 16, 1997

Rejection at Issue

Claims 1, 2, 4 through 6, 7, 8 and 10 through 12 stand rejected under 35 U.S.C. § 103 as being obvious over Burr. Claims 3 and 9 stand rejected under 35 U.S.C. § 103 as being obvious over Burr in view of Warashina. Throughout the opinion we make reference to the briefs and the answer for the respective details thereof.

Opinion

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

With full consideration being given to the subject matter on appeal, the examiner's rejections and the arguments of appellants and the examiner, and for the reasons stated *infra* we will not sustain the examiner's rejection of claims 1 through 12 under 35 U.S.C. § 103.

On page 8 of the brief appellants argue:

> *Burr* merely discloses a fully depleted SOI device in which the depletion region 328 extends completely down to the interface of the oxide layer 308. Thus, nothing in *Burr* shows, teaches or suggests a surrounded body or region including a depletion layer having a composition surface which is in contact with the insulating layer as claimed in claims 1, 6, 7, and 12. Rather, *Burr* merely discloses a depletion region 328.

Further, appellants assert:

> *Burr* merely discloses controlling the threshold voltages in accordance with the substrate bias. However, as claimed in claims 1, 6, 7, and 12, a voltage of a first polarity applied to the substrate of the EIB-MOS transistor induces charges of a second polarity over the composition surface of the surrounded or body region.

In response, on page 6 of the answer, the examiner states:

> The Examiner takes the position that the two statements included in the above quote [referring to a quote from page 9 of appellants' specification which we omit] namely "electrons are introduced into the substrate 20" and "a p type neutral region which is not present in the conventional fully depleted SOI MOS transistor is provided in the body electrically," are statements of applicants' particular theories concerning the physics of the device and do not define structure. For this reason the Examiner concluded that Applicant defines EIB and EIB-MOS as an SOI MOS transistor having a structure which is adapted for the application of a negative voltage V_{sub} to the substrate.

In the Reply brief, on page 3, appellants further clarify the differences between Burr and the claimed invention, stating:

> In particular, the novel and unique feature of the invention claimed in claims 1-12 is that a p-type neutral region (i.e. holes) is induced in the body 26 by applying a voltage to the substrate. On the other hand, in a fully depleted SOI-MOS transistor, the composition surface is depleted such that holes do not occur even though a voltage is applied (which is why it is called a fully depleted SOI MOS). The reason that holes cannot be introduced in the fully depleted SOI MOS is because no carriers exist within the body since the body is fully depleted.

We concur with the appellants. Claim 1 includes the limitation "comprising an EIB-MOS transistor of which said substrate is adapted to be applied with a voltage of a first polarity for inducing charges of a second polarity over said composition surface of the surround region." Thus, claim 1 requires a

transistor where a charge applied to the substrate will induce a charge over the composition surface of the surround region. Independent claims 6, 7 and 12 contain similar limitations. While this limitation does not directly define the structure of the device, it does define a quality of the structure.

We find that Burr teaches a SOI device in which the threshold can be tunable. See column 3, lines 7 to 13. Burr's device is of similar architecture to appellants in that Burr teaches (viewing figures 5 and 6) a substrate (510, 610), an insulating layer (508, 608), a single crystal layer with a source (512, 612), a drain (514, 614) and a surrounded region (516, 616). We find that Burr teaches that a bias is applied to the insulating layer (544, 654). See column 2, lines 54-57 and column 6, line 44-47. We find that Burr teaches that the surrounded region is a fully depleted region. Burr teaches that the term, "fully depleted" means that the depletion region extends completely down to the interface with the oxide layer. See column 1, lines 48-50. We concur with appellants' assertion that because the surrounded region is fully depleted, a charge cannot be induced in the region. The term "depletion region" is defined as "the portion of the channel in a metal oxide field effect transistor in which there are no charge carriers."[2] As there are no charge carriers in the surrounded, fully depleted region, we find that when a bias is applied to the transistor of Burr, a charge will not be induced on the composition surface of the surrounded region. Further,

[2] Definition taken from McGraw-Hill Dictionary of Scientific and Technical Terms, Fifth Edition, 1994.

we find that Burr's teaching of biasing the insulating layer is limited to fully depleted transistors as Burr recognizes that partially depleted transistors can be made tunable by using an ohmic contact between the gate and a bulk contact. See column 2, lines 10 to 13. Thus, we find that Burr neither teaches nor suggests the claimed limitation of "said MOS transistor comprising an EIB-MOS transistor of which said substrate is adapted such that when a voltage of a first polarity is applied, charges of a second polarity are included over said composition surface of the surround region." Accordingly, we will not sustain the examiner's rejection of claims 1, 2, 4 through 6, 7, 8 and 10 through 12 under 35 U.S.C. § 103 as being obvious over Burr.

We next consider the examiner's rejection of claims 3 and 9 under 35 U.S.C. § 103 as being obvious over Burr in view of Warashina. Claims 3 and 9 depend upon claims 1 and 7. The examiner does not assert, nor do we find that Warashina teaches or suggests modifying Burr such that a bias on the substrate will induce charge on the composition surface. Accordingly, we will not sustain the examiner's rejection of claims 3 and 9 under 35 U.S.C. § 103 as being obvious over Burr in view of Warashina for the reasons discussed supra with respect to claims 1 and 7.

In summary we will not sustain the examiner's rejections under 35 U.S.C. § 103. Accordingly, we reverse the examiner's rejection of claims 1 through 12.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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HOWARD B. BLANKENSHIP) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
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ROBERT E. NAPPI)
Administrative Patent Judge)

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BURNS, DOANE, SWECKER & MATHIS, L.L.P
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404